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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

JOZEF D. MITROS ET AL.

Serial No. 10/020,034 (TI-32931)

Filed December 7, 2001

For: METHOD FOR FABRICATING LOW CHC DEGRADATION MOSFET TRANSITSORS

Art Unit 2823

Examiner Long Pham

Customer No. 23494

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Jay M. Cantor, Reg. No. 19,906

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 18, 19, 26 and 27, all of the rejected claims. Claims 1 to 17, 20 to 25 and 28 to 30 have been allowed. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

An amendment was filed after final rejection and was entered for purposes of appeal.

SUMMARY OF INVENTION

Many applications for integrated circuits require that both relatively high and relatively low voltage MOSFETS be fabricated on the same chip. It is also a continual goal in the art to fabricate semiconductor devices utilizing fabrication procedures having a minimum number of steps in order to maximize yield and economics. The present invention provides such a solution for the fabrication of an integrated circuit having both relatively high voltage and relatively low voltage transistors thereon, both of which can be of the same conductivity type.

The invention which accomplishes the above-described goal relates to a method of fabricating MOSFET transistors in a semiconductor device wherein the threshold voltage of a relatively low voltage first transistor in a first region of a semiconductor device substrate is adjusted concurrently with the formation of a source/drain region of a relatively high voltage second transistor, both using the same implant. This is shown in step 24 in Fig. 1a as discussed at page 8, lines 10 to 25 and a specific embodiment of this feature is discussed at page 10, line 20 to page 11, line 2 with reference to Fig. 2.

ISSUES

The issues on appeal are as follows:

1. Whether claims 18 and 19 are patentable over Lin et al. (U.S. 6,297,082) in view of Nakahara (U.S. 5,075,242) under 35 U.S.C. 103(a).

2. Whether claims 26 and 27 are patentable over Lin in view of Nakahara under 35 U.S.C. 103(a).

GROUPING OF CLAIMS

Claim 19 stands or falls with claim 18 and claim 27 stands or falls with claim 26.

ARGUMENT

ISSUES 1 and 2

Claims 18, 19, 26 and 27 were rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. 6,297,082) in view of Nakahara (U.S. 5,075,242). The rejections are without merit.

Claim 18 provides a method of semiconductor fabrication wherein source/drain regions in one high voltage transistor are implanted using a threshold voltage adjust implantation which is concurrently also being used to adjust the threshold voltage of another relatively low voltage transistor. This is set forth in claim 18 by the language adjusting a threshold voltage of a first transistor relatively low voltage device in a first region of said semiconductor device substrate and, concurrently with the step of adjusting, forming a source/drain region of a second transistor relatively high voltage device, both using the same implant. Clearly, Lin et al. does not teach or suggest the problem or the solution thereof as admitted in the Office action. In fact, the Examiner

states that Lin adjusts the threshold voltage of the low voltage device with a different implantation than is used to form the source/drain region of the high voltage device. Nakahara also fails to teach or suggest the above-described concept, even were Nakahara to be combinable with Lin et al., which it is not. In fact, Nakahara does not even discuss fabrication of a semiconductor device wherein concurrent fabrication steps for fabrication of a relatively high voltage transistor and a relatively low voltage transistor are provided. The fact that a pair of opposite conductivity-type (as opposed to a high voltage and low voltage device) devices are fabricated using a concurrent implantation has nothing whatsoever to do with the problem solved by the claimed invention. It follows that there are no fabrication steps involving the specific types of fabrication steps claimed. Furthermore, as stated above, there can be no teaching or suggestion to combine the references when neither reference even teaches or suggests the problem solved by the present invention, let alone the solution thereto.

In the Advisory Action, the Examiner states:

> "Nakahara broadly teaches forming source/drain region of a MOS and adjusting the threshold voltage of another MOS by a single implantation"

While this statement is correct, it has nothing whatsoever to do with the formation of a relatively high voltage transistor concurrently with a relatively low voltage transistor. The fact that Nakahara utilizes a step similar to that claimed for an entirely different purpose has nothing whatsoever to do with reasons for utilizing this step as claimed herein. The only basis for utilizing the step taught in Nakamura in the invention claimed herein is the teaching of the subject disclosure. Nowhere is there even an iota of a teaching or suggestion in Nakamura or Lin et al. to use the step of "adjusting a the

threshold voltage of a first transistor relatively low voltage device in a first region of said semiconductor device substrate; and concurrently with said step of adjusting, forming a source/drain region of a second transistor relatively high voltage device, both using the same implant" as required in claim 18 or "selectively concurrently implanting a first relatively low voltage transistor region in said semiconductor device substrate to adjust ~~a~~ the threshold voltage associated with a first transistor device and implanting a portion of a second transistor region to form a source/drain region associated with a second relatively high voltage transistor device" as required in claim 26. The mere fact that a step in a first process is similar to a step in a totally different second process does not make it obvious to use that step in the second process. Clearly, there is no teaching or suggestion to utilize the step as claimed in the process of the appealed claims in an environment wherein transistors, even of the same conductivity type, can be fabricated having different operating voltages and using the common step.

Claim 26 requires, among other steps and as stated above, the steps of selectively concurrently implanting a first relatively low voltage transistor region in said semiconductor device substrate to adjust a threshold voltage associated with a first transistor device and a portion of a second transistor region to form a source/drain region associated with a second relatively high voltage transistor device. The arguments presented above with reference to claim 18 apply and are incorporated by reference.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,

Jay M. Cantor
Reg. No. 19906
(301) 424-0355

APPENDIX

The claims on appeal read as follows:

18. A method of fabricating MOSFET transistors in a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

adjusting a the threshold voltage of a first transistor relatively low voltage device in a first region of said semiconductor device substrate; and

concurrently with said step of adjusting, forming a source/drain region of a second transistor relatively high voltage device, both using the same implant.

19. The method of claim 18, further comprising the step of forming a source/drain region of the first transistor device.

26. A method of forming a source/drain region in a semiconductor device, comprising the steps of:

providing a semiconductor device substrate; and

selectively concurrently implanting a first relatively low voltage transistor region in said semiconductor device substrate to adjust a the threshold voltage associated with a first transistor device and implanting a portion of a second transistor region to form a source/drain region associated with a second relatively high voltage transistor device.

27. The method of claim 26, wherein selectively implanting the first transistor region and a portion of the second transistor region comprises the step of implanting one of phosphorus, arsenic and boron in the first transistor region and a portion of the second transistor region.